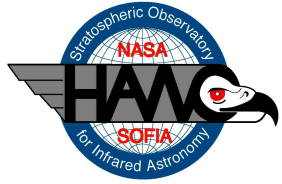


# Detector Subsystem Update

Dr. Harvey Moseley  
GSFC Lead Co-Investigator



## Detector preliminary design has matured since PDR

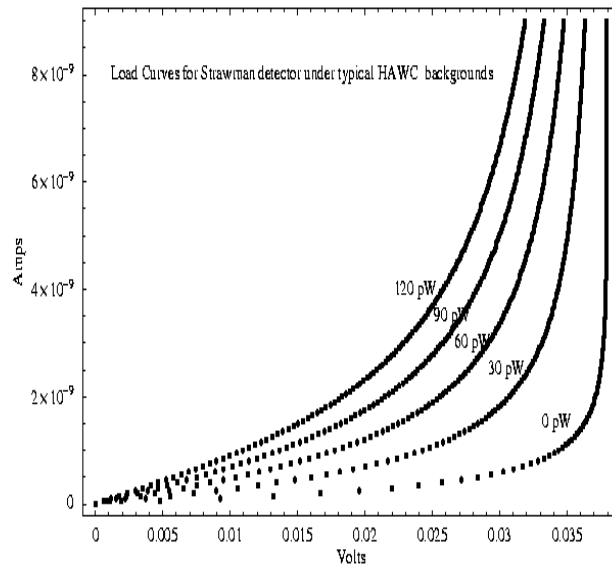


- Key design decisions have been made since PDR, based on flowdown of system requirements:
  - Broadband coating
  - Full-area thermometer
  - 4.2 K load resistors
  - 120K JFET operating temperature
- HAWC assembly prototype fabricated
- SPIRE detector thermal design verified by test
- Design and manufacturing lessons learned from SPIRE are being incorporated into HAWC design



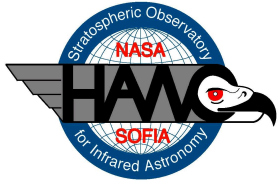
# Detector thermal properties chosen

hwrep02.nb



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- $G(T)$ ,  $R(T)$  have been chosen
- $G(T) = 6.3 \times 10^{-9} T^3$
- $R(T) = 700 e^{-\sqrt{28/T}}$



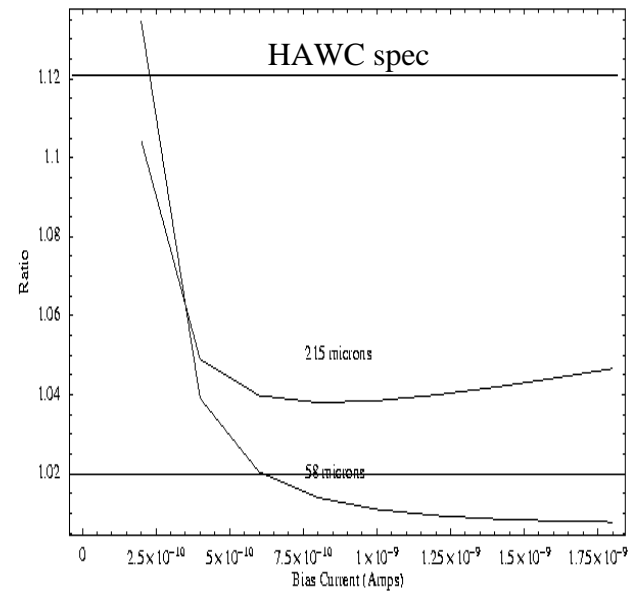
# Detector sensitivity exceeds requirements in all 4 bands



- Detectors perform well in all bands with a single selected bias

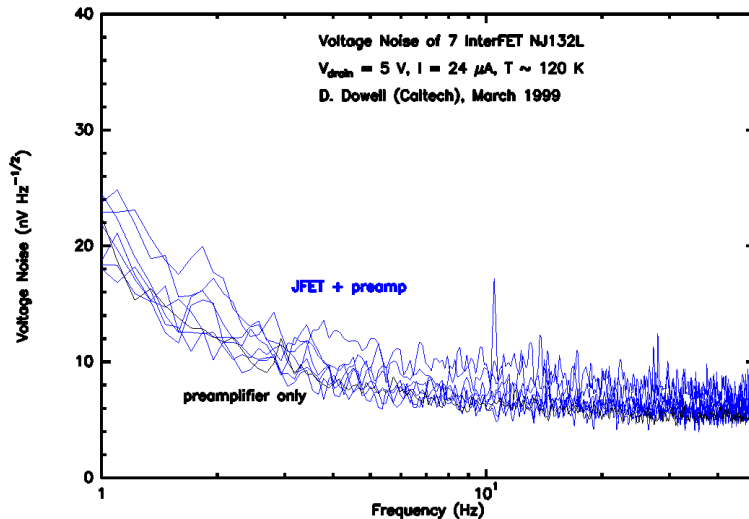
hmcyp@2.nb

1

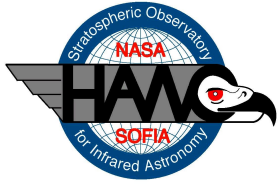




# JFET noise meets requirements



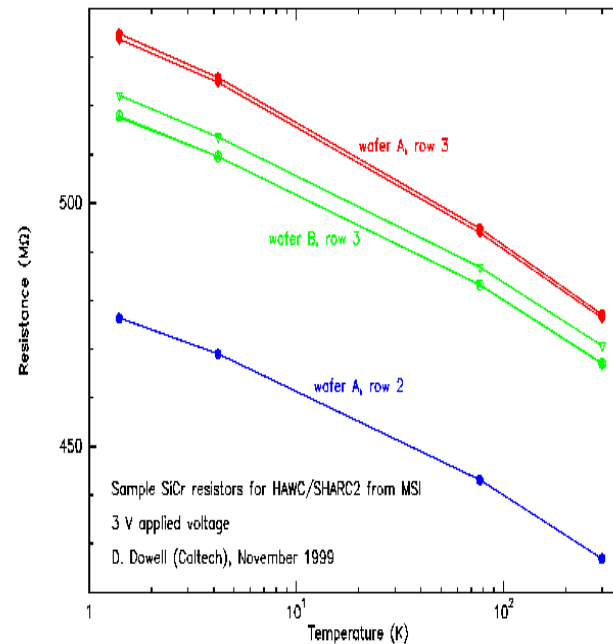
- Testing conducted by Dr. Darren Dowell at CalTech 3/99 and 11/99
- Both (commercial) InterFET and (custom) GSFC designs have now been tested at range of temperatures
  - Baseline choice: InterFET
  - Backup: GSFC
- Both designs have good performance at their respective design operating temperatures
  - InterFET (baseline choice): 120 K
  - GSFC: 77K



# Sichrome Load Resistor samples tested

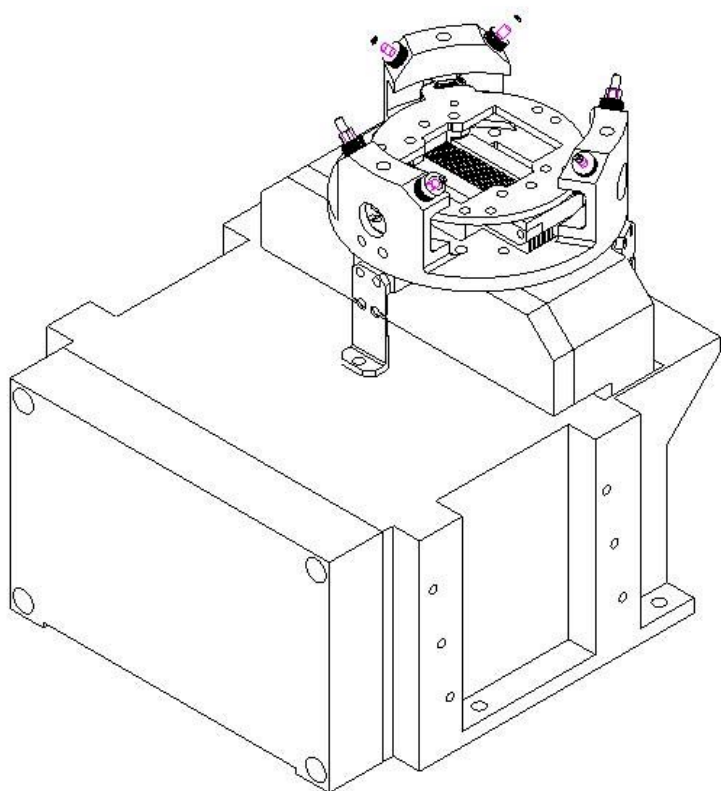


- Tests conducted by Darren Dowell in 11/99
- Results
  - Temperature behavior consistent between all test samples
  - No significant variation in resistance with voltage except for cold temps and  $V > 10$  V (self-heating)





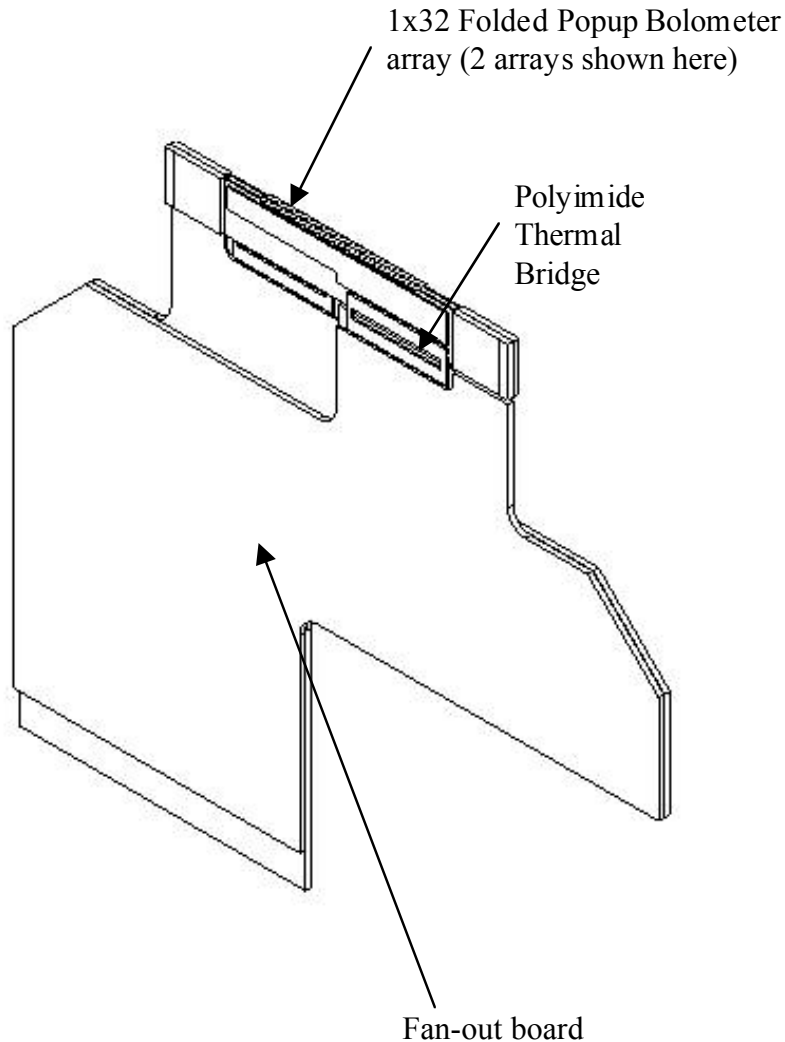
# Promising hardware development means baseline detector specifications have been maintained



- FPA:
  - Technology: Ion-implanted pop-up silicon bolometers
  - Large array format: 12x32 pixels (384 total);
    - Pixel size: 1.000 mm  $\pm$  0.004 mm (x-direction);  $\pm$  0.025 mm (y-direction, goal 0.010 mm)
    - Detector row spacing: 1.000  $\pm$  0.025 mm
  - Operating temperature: 200 mK
- JFETs:
  - InterFET (NJ132L) JFETs operating at 120K
- Load Resistors
  - Sichrome operating at 4.2 K (located in JFET box)



# Revised detector card design incorporates lessons learned



- Each Detector Card consists of:
  - 1 x 32 “folded” array of Pop-up Detectors
  - Polyimide Thermal Bridges
  - Fan-out board
- Detector cards now assembled as a “left-handed” and “right-handed” pair

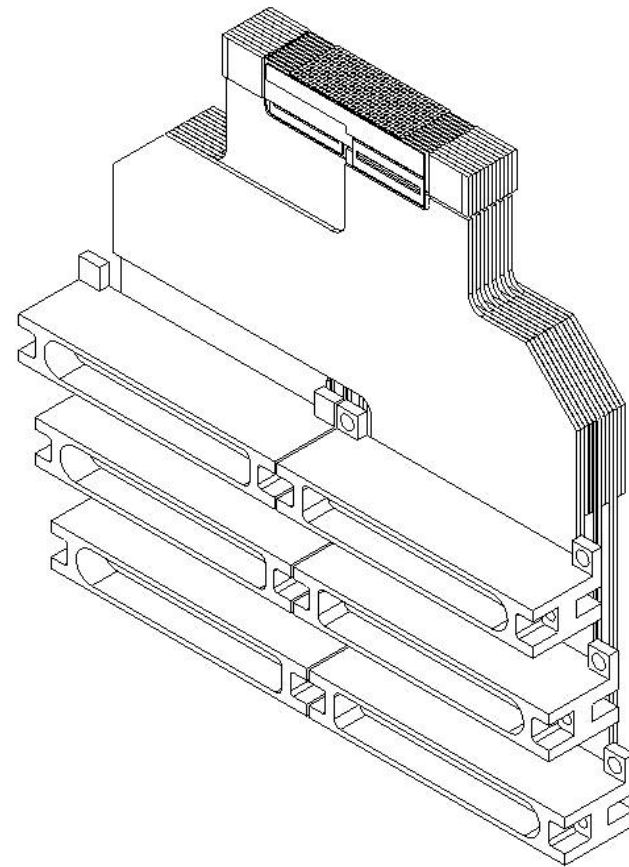


# Simplified detector card assembly



12 x 32 “stacked” array

- Motherboard eliminated, edge mounted connectors on cards plug directly into JFET box
- Compact design allows card cage to be eliminated





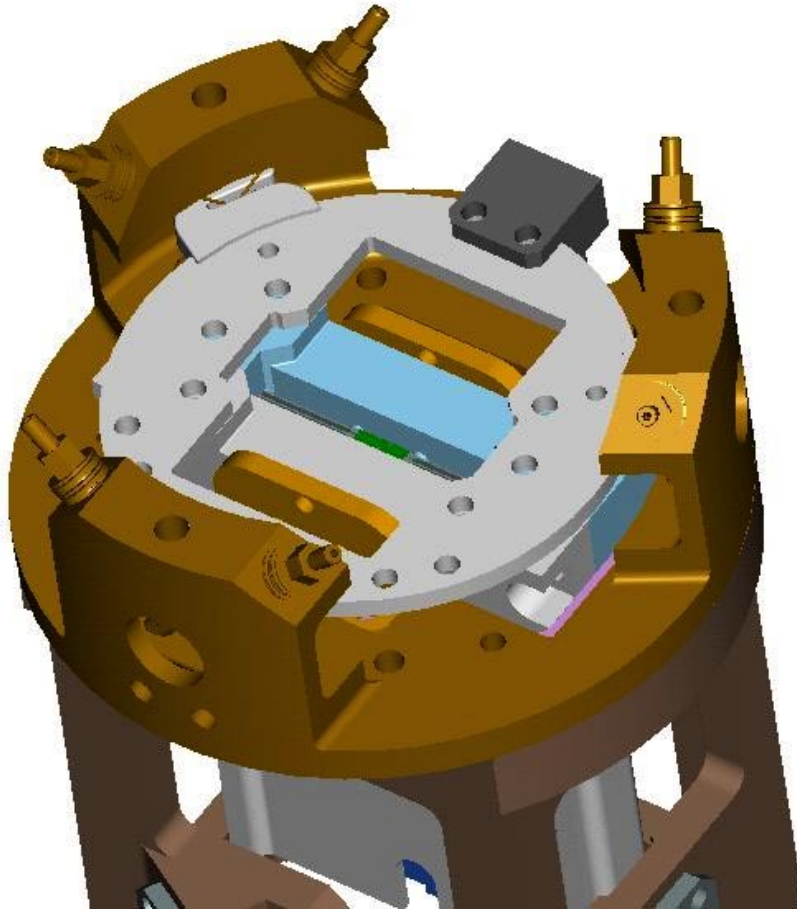
Lessons learned during SPIRE development are directly transferable to HAWC design and integration



- Materials
- Thermal design
- Detector assembly integration
- Software development
- Test facilities and equipment



# Detector assembly prototype confirms design concepts





## GSFC is continuing to reduce detector development risk



- Identified Risk areas which are still being mitigated:
  - Kevlar creep
  - Schedule
  - Microphonics
  - Yield



# Detectors ready to move from preliminary to final design



- Design requirements defined
- Key design decisions have been made
- JFETs have been procured and screened
- Load resistors have been tested
- Incorporating lessons learned from HAWC prototype and SPIRE development