

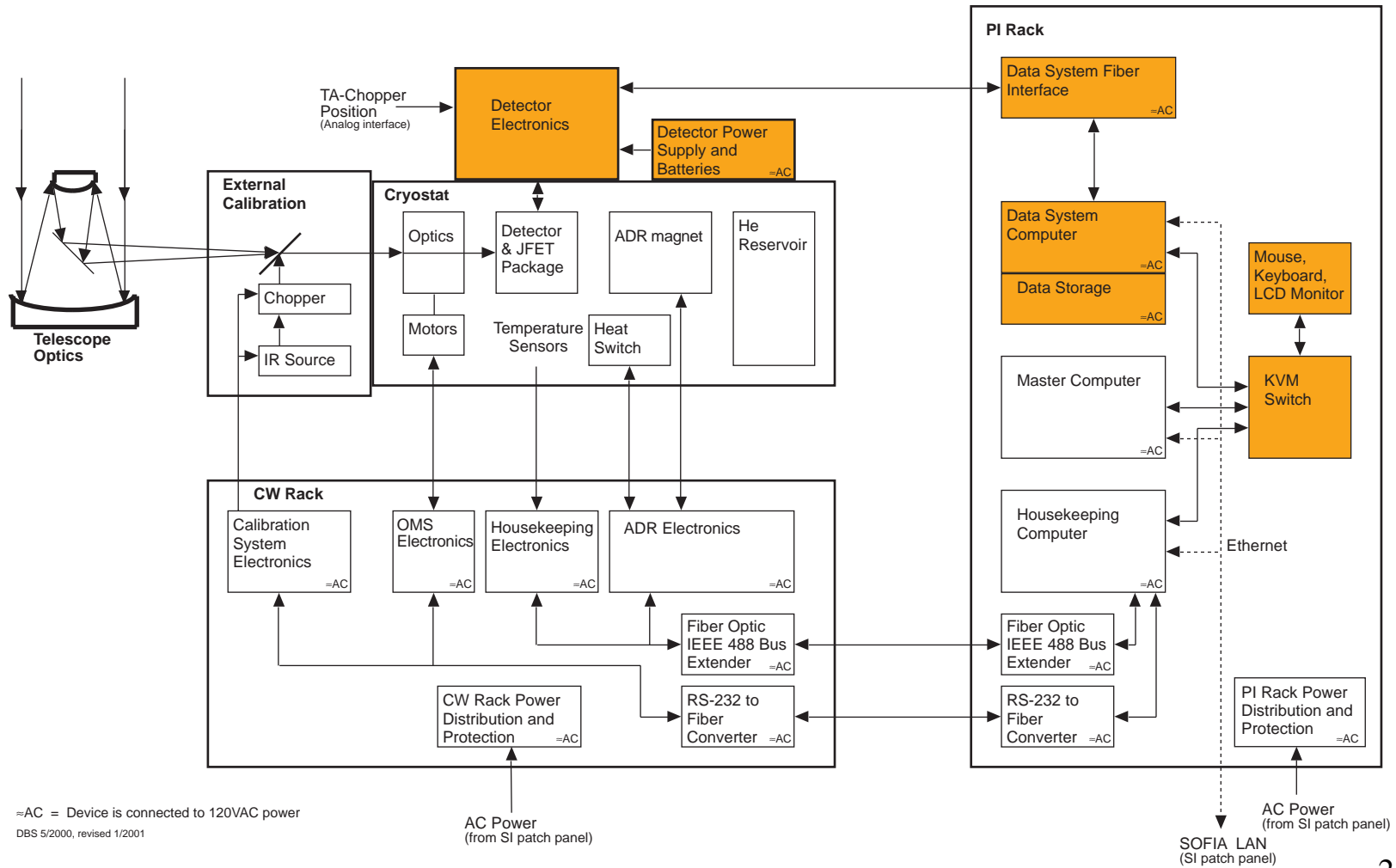
HAWC CDR

February 1-2, 2001

Data Electronics

Dale Sandford

HAWC Electronics Overview





Requirements



- **Digitize AC signals from 32x12 detector array**
 - Sample rates from 1KHz to 4KHz
- **Digitize DC detector bias**
- **Supply JFET power and detector bias voltage**
- **Control JFET temperature**
- **Interface with SMA and calibration systems for chopping synchronization**
- **Interface with Instrument Control System**



Relevant ICDs



- **Detector/JFET module**
 - (3) 304-pin Packard-Hughes connectors
 - Pinout finalized 12/15/00
- **Telescope cabling (TA_SI_01)**
 - AC power
 - Fiber optics
- **SOFIA SMA (TA_SI_04)**
 - (2) analog input for chopper position
 - (1) digital input for waveform synchronization
 - (2) analog outputs for waveform generation
 - (1) digital output for waveform synchronization
- **Calibration system**
 - parallels interface to SMA
- **Instrument Control System**
 - Communication through ethernet LAN
 - Draft protocol completed



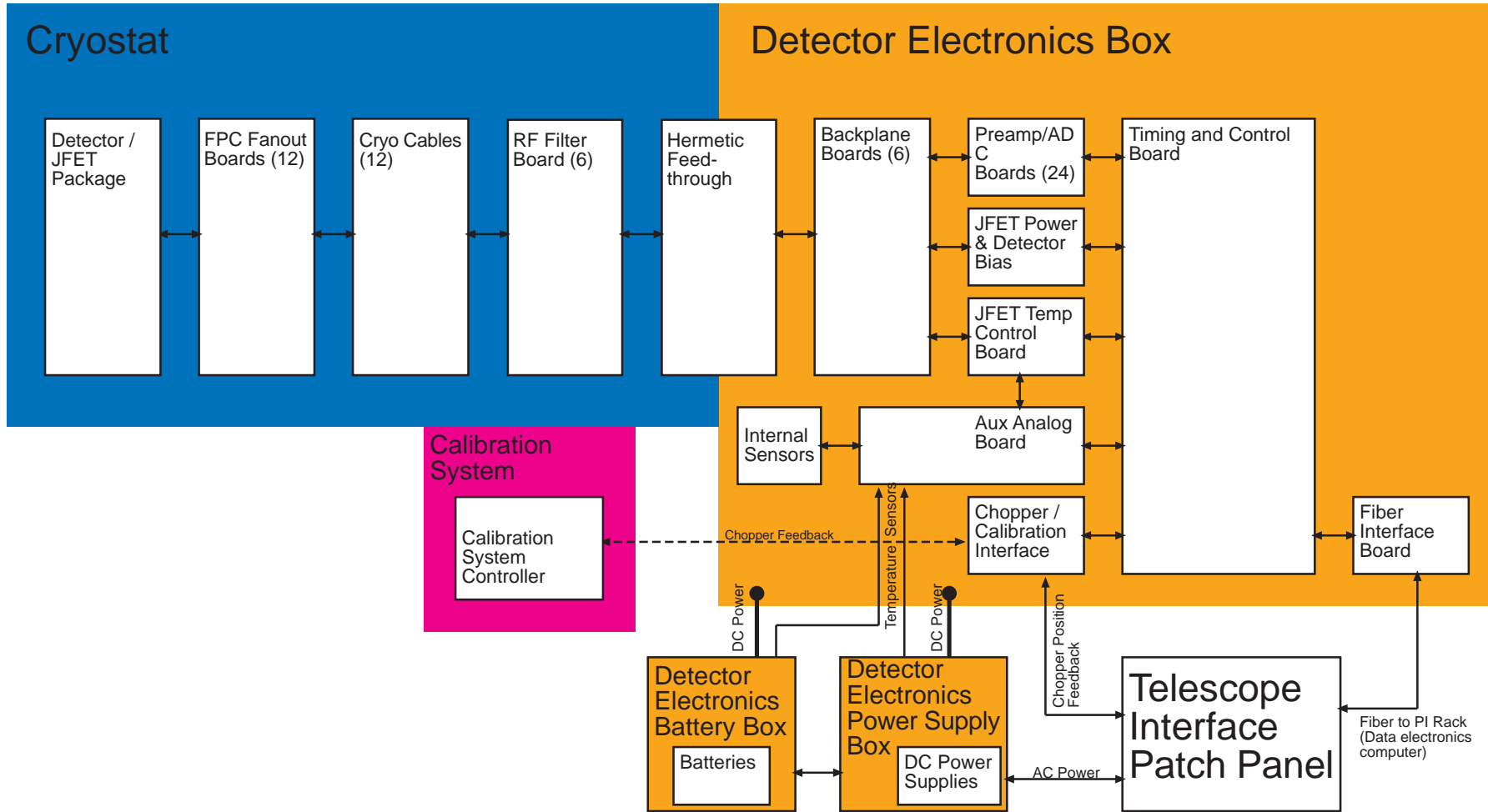
Changes Since PDR



- **Preamp/ADC**
 - Changed from Crystal ADC to Burr-Brown ADC with integral programmable gain.
- **Host computer fiber interface**
 - Computer fiber interface will now use two National instrument parallel cards instead of one. This change simplifies both hardware and software implementation.
 - Physical fiber link changed from AMD TAXI chipset to Agilent (HP) chipset.



Overview





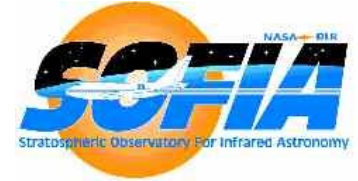
System Components



- **Signal cabling (Cryostat interior)**
 - Flexible printed circuit board from JFET drawers to dewar cabling
 - Cryo cabling (TekData)
 - RF filter board at dewar entry
 - Hermetic connectors (Hermetic Seal Corp.)
- **Detector electronics box (Cryostat exterior)**
 - (6) Backplane boards
 - (24) Preamp/ADC boards
 - Timing and control board
 - Chopper and Cal source interface board
 - Fiber interface board
 - JFET power and detector bias board
 - JFET temperature control board
 - Auxiliary analog board

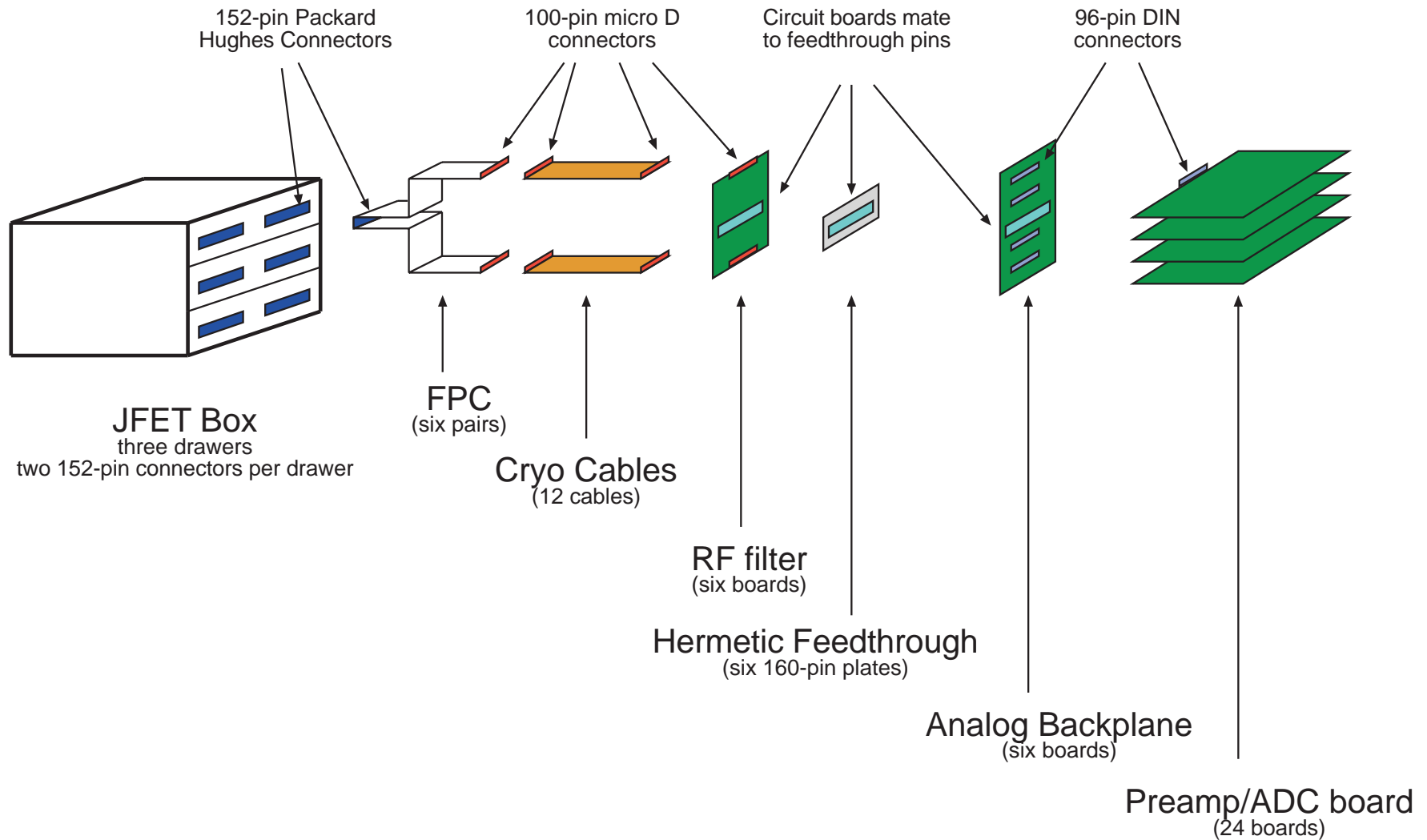


System Components (Cont.)



- **Detector electronics power supply box (Cryostat exterior)**
 - AC power filtering, fuses, etc.
 - Linear power supplies
- **Detector electronics battery box (Cryostat exterior)**
 - (2) 6V 33Ah sealed lead acid batteries
 - (2) 6V 3Ah sealed lead acid batteries
 - Battery power interruption relay
- **Computer fiber interface (PI rack)**
 - Fiber interface board
 - Power supply
- **Host computer (PI rack)**
 - (2) National Instruments DIO-32HS PCI cards
 - Raw data disk storage (optional)

Detector Cabling





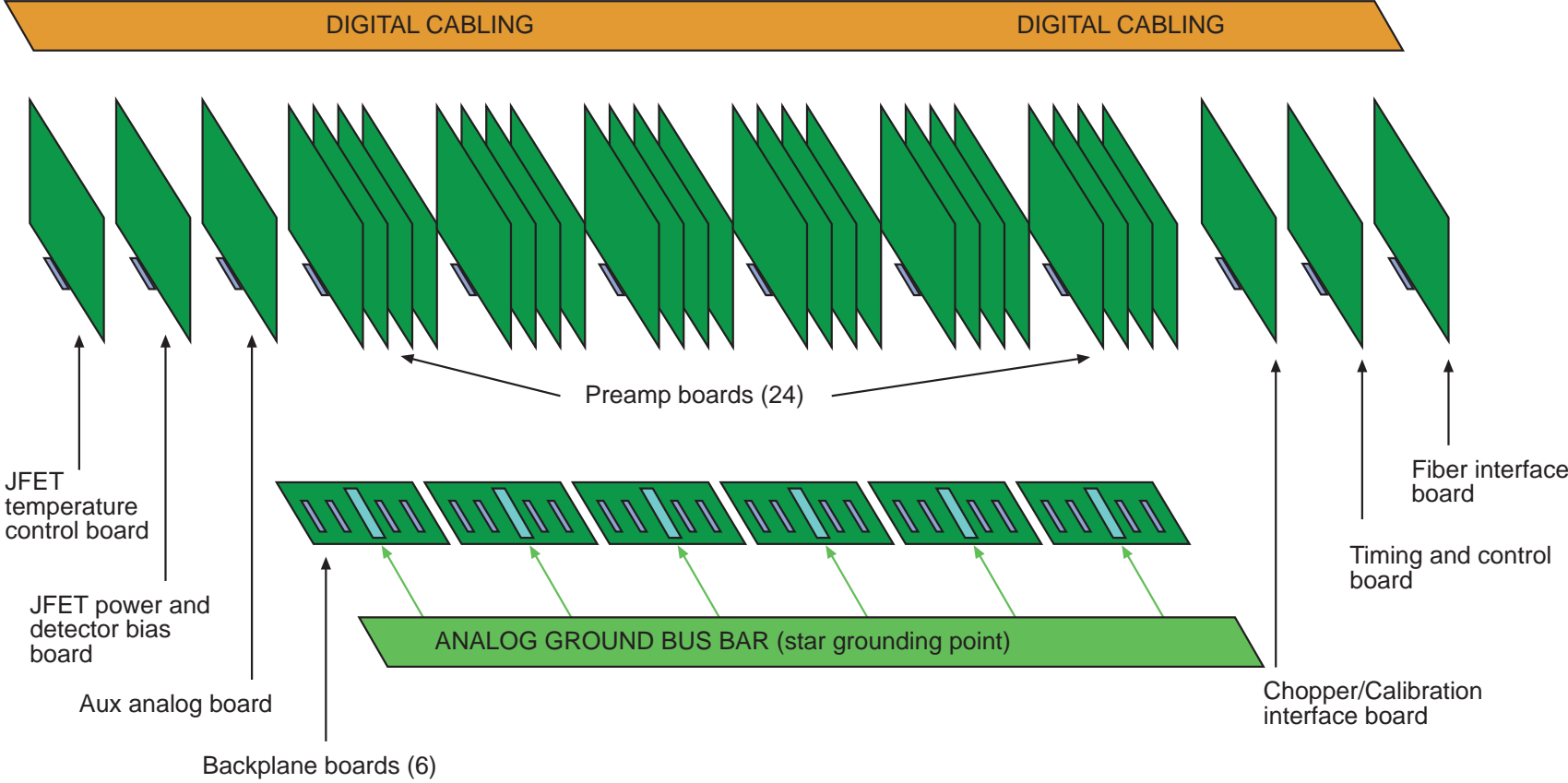
Detector Electronics Box



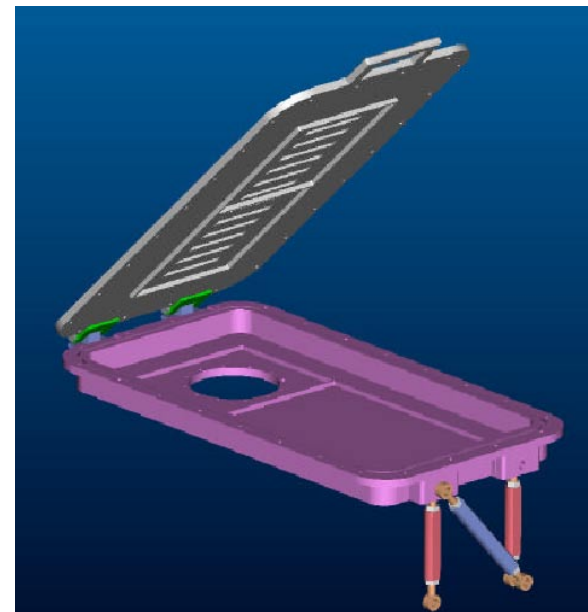
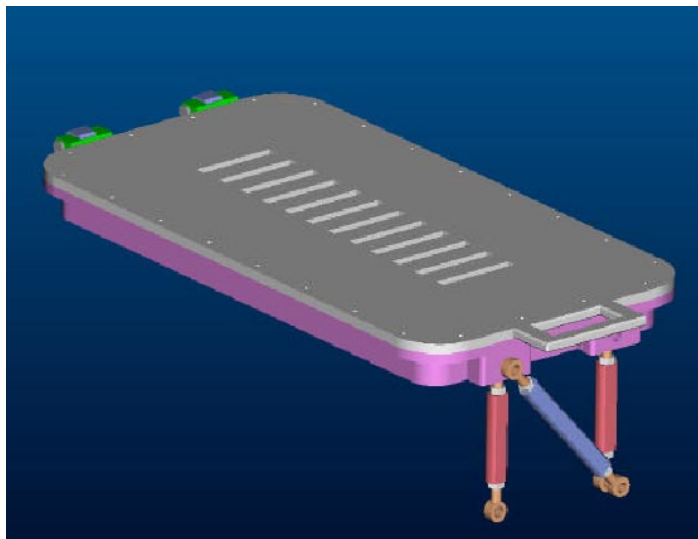
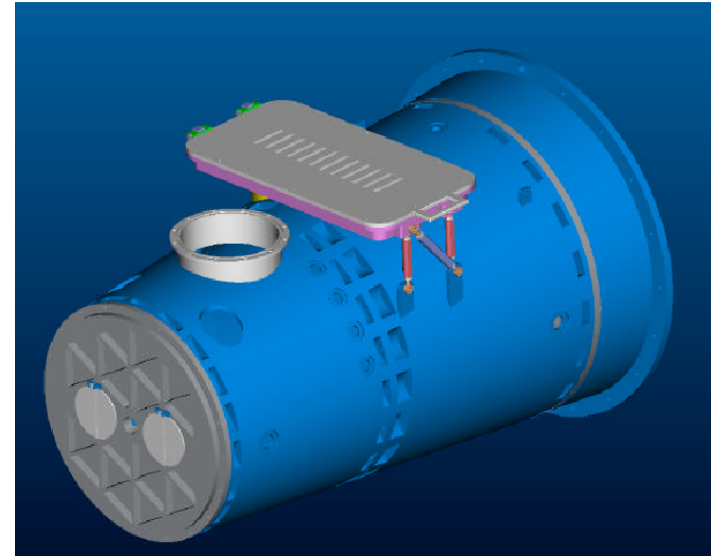
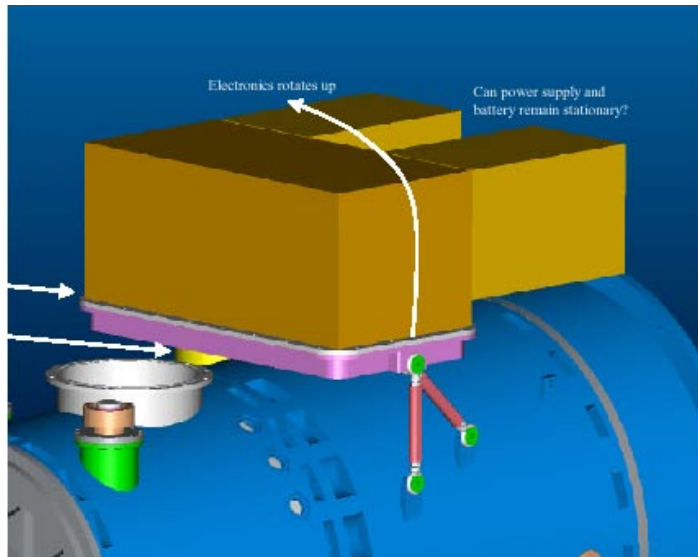
- **Card cage structure**
 - Preamp/ADC boards plug into backplane boards
 - Backplane boards connected to hermetic connectors
 - Shielding between boards
 - 30 circuit boards on 0.8 inch centers
 - RF filtering on all copper connections into box
- **Power supplied by Detector battery and power supply boxes**
- **Mounted to cryostat exterior**
 - Box structure and mounts designed for airworthiness loads



Box Layout

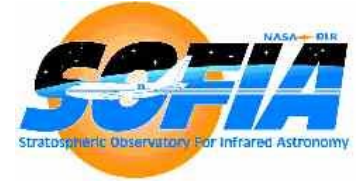


Box Mount & Feedthrough



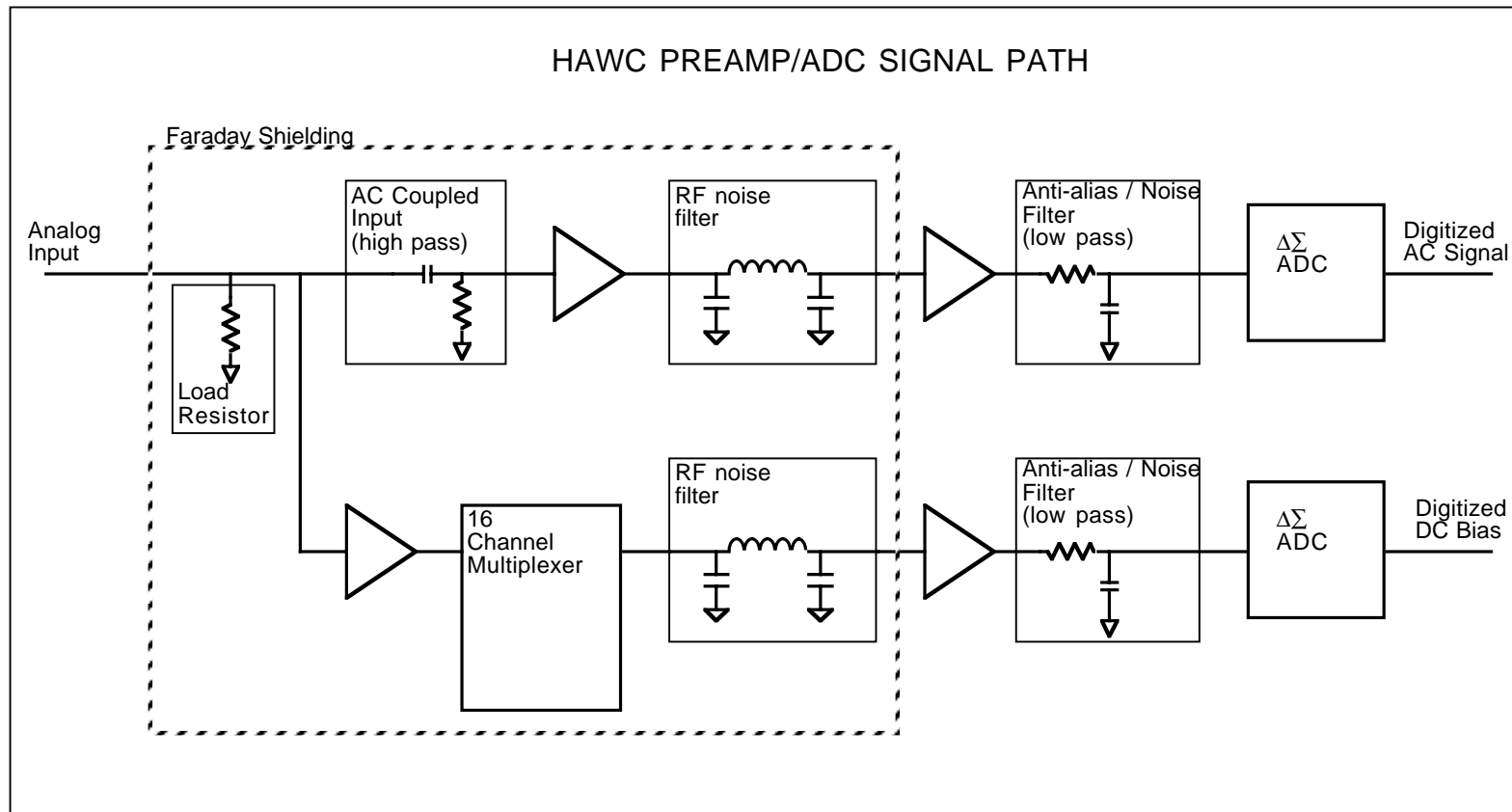


Preamp/ADC Board



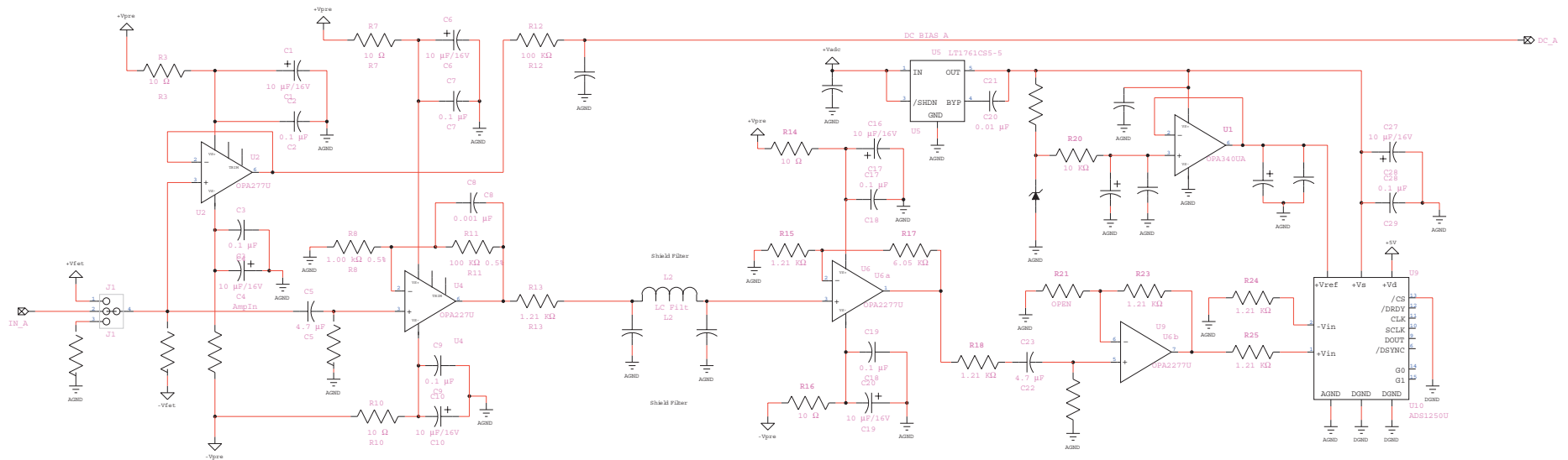
- **Each board handles 16 bolometer channels**
- **Preamp**
 - Preamp enclosed in Faraday cage on board
 - AC and DC signal paths buffered separately
 - First stage of AC and DC preamps powered by battery
- **RF filters**
 - Pi LC filter between ADC and first stage preamp at Faraday shield
- **ADC**
 - Individual ADC for each AC signal
 - One multiplexed ADC per board for DC bias signals
 - 20-bit Burr-Brown delta-sigma ADC
- **Analog signals enter at “bottom” of board**
- **Digital signals enter/exit at “top” of board**

Signal Chain



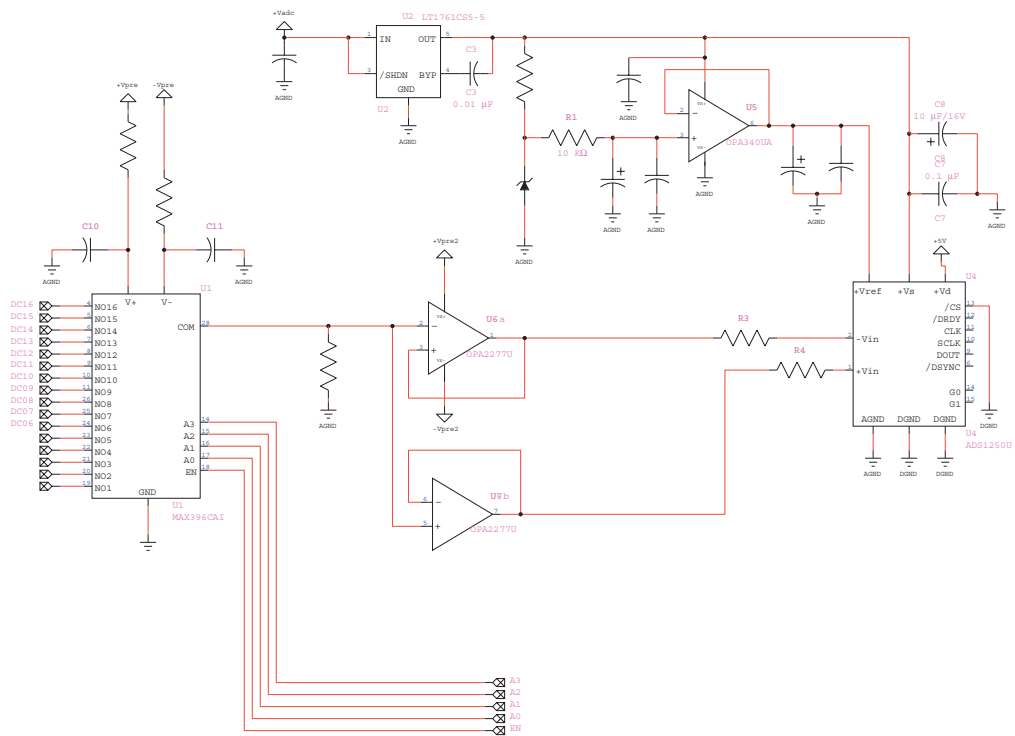


Preamp /ADC Schematic Excerpt

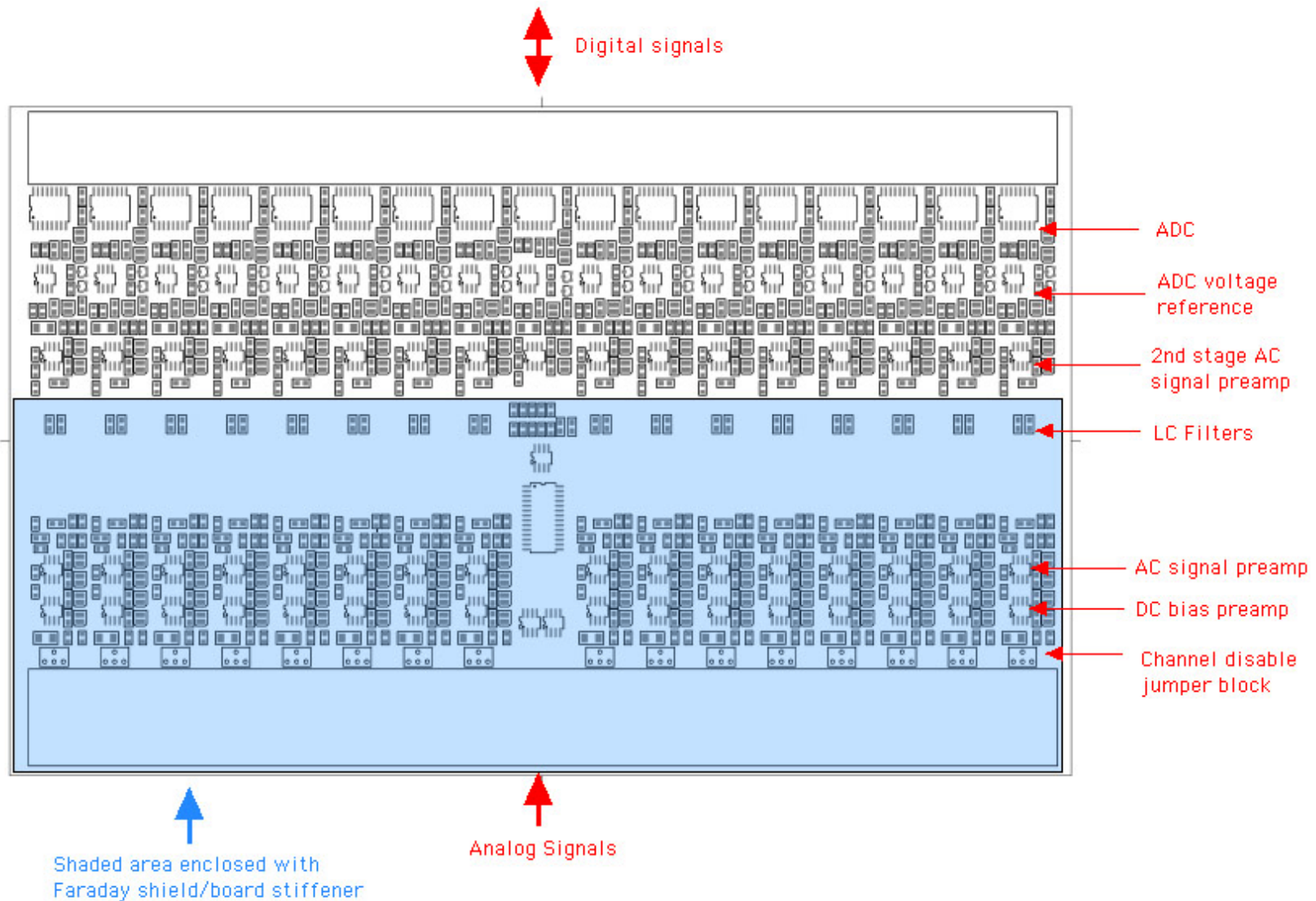




DC Mux Schematic Excerpt

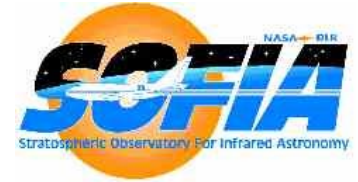


Preamp/ADC Layout





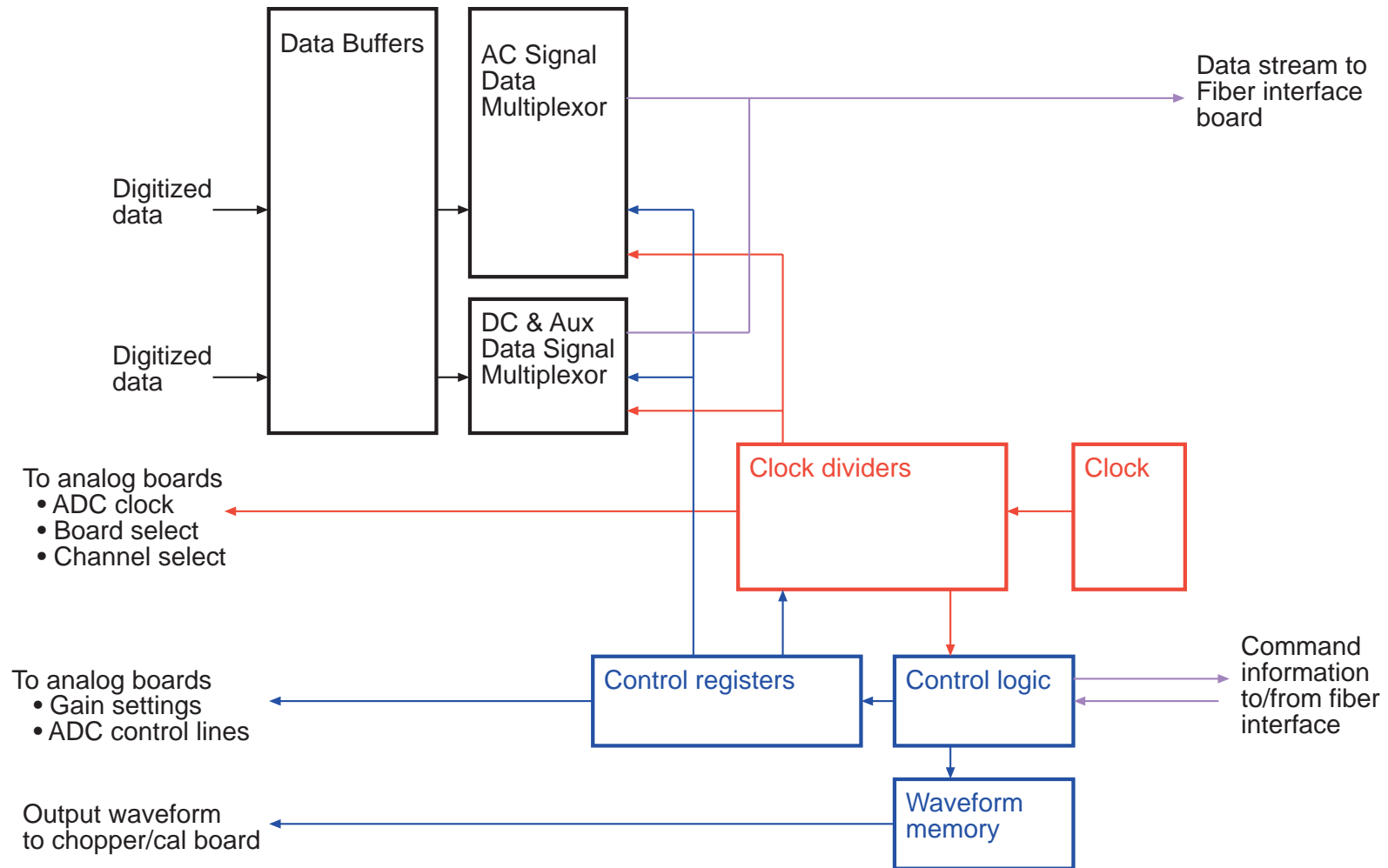
Timing and Control



- **Provides clocking for ADC**
 - All ADCs run from same master clock
 - Master clock allows sample rates from 1KHz to 4KHz
- **Buffers and multiplexes digital data stream**
- **Control implemented in state machine**
 - Start/stop data conversion
 - Set signal path gains
 - Can select DC bias signal channel
 - Set master clock speed (divider)

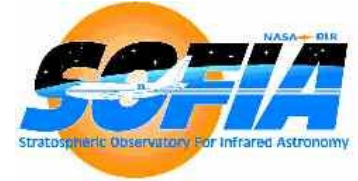


Timing and Control Board





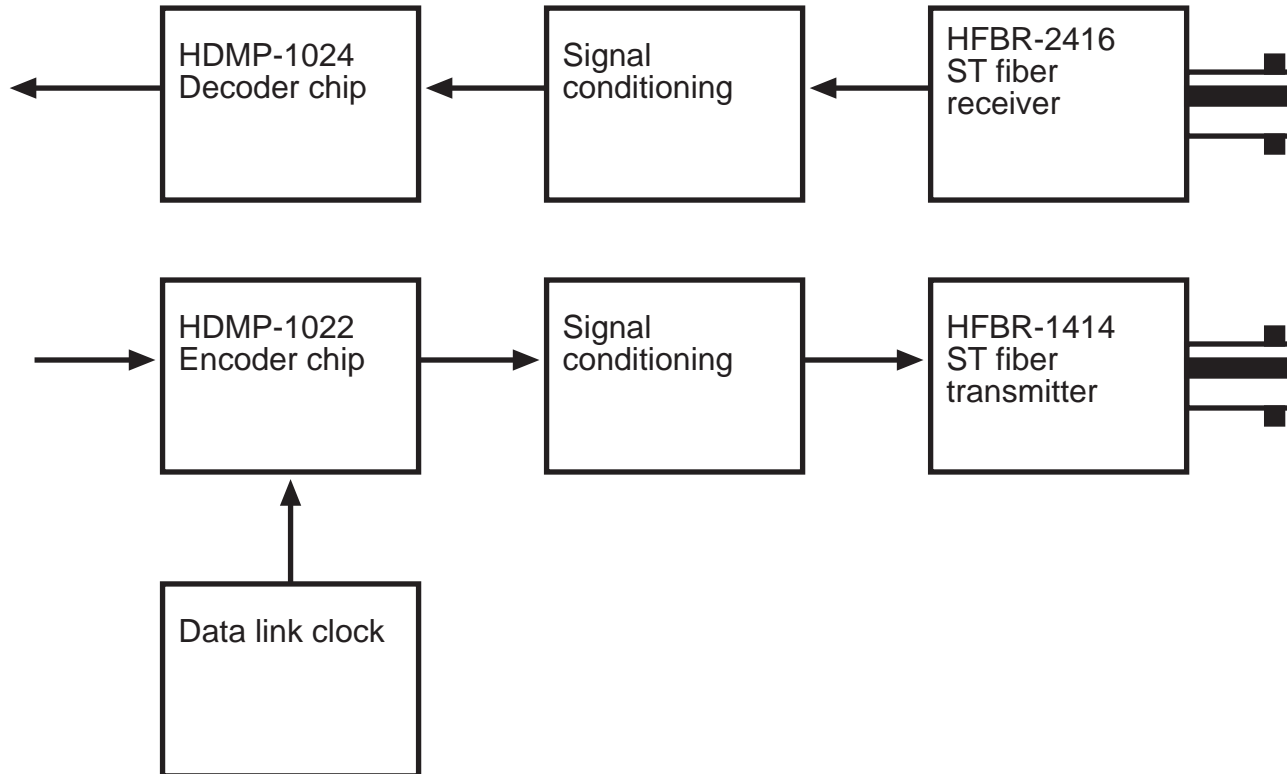
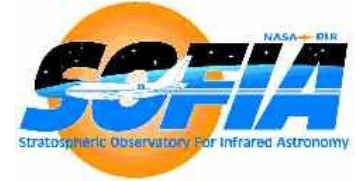
Fiber Interface



-
- **Provides electrical isolation between data electronics and computers**
 - Requires two optical fibers
 - **Uses Agilent encoder/decoder chipset**
 - HDMP-1024 decoder
 - HDMP-1022 encoder
 - **Uses Agilent fiber transmitter and receiver**
 - HFBR-2416 receiver
 - HFBR-1414 transmitter
 - **150 Mbaud data link**
 - 20-bit words
 - 7.5 M words/sec



Fiber Interface Board





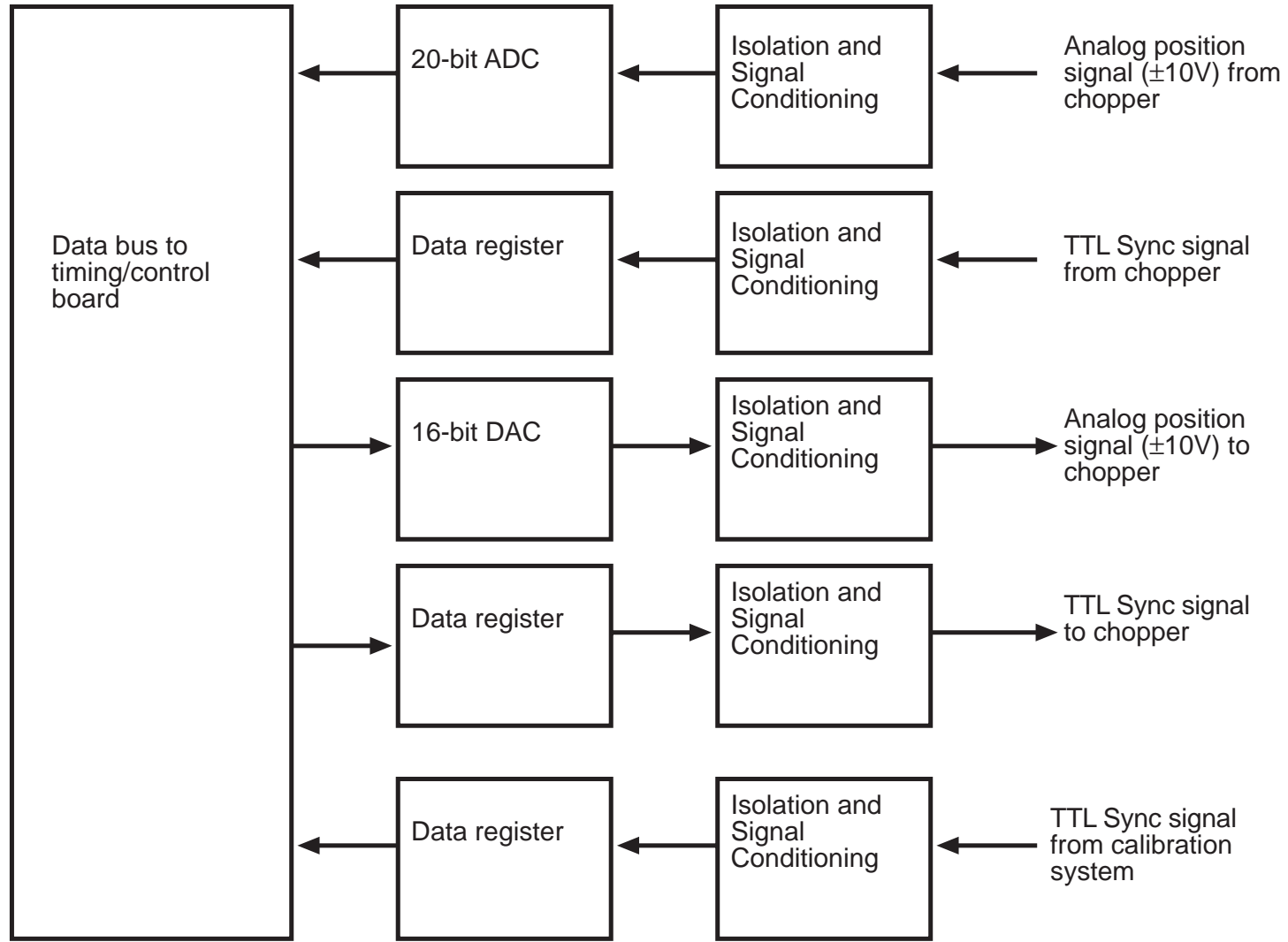
Chopper/Cal Interface



- **Interface to SMA per TA_SI_04**
 - Signals from chopper are recorded synchronously with balometer data
 - Chopper X,Y analog position signals
 - Chopper digital sync signal
 - Can provide signal for driving chopper
 - X, Y waveform generated by 16-bit DACs
 - Waveform data stored in RAM on timing/control board
 - Waveform generation synchronized to balometer data stream
- **Interface to calibration system**
 - Chopper sync pulse recorded synchronously with data stream



Chopper/Cal Board





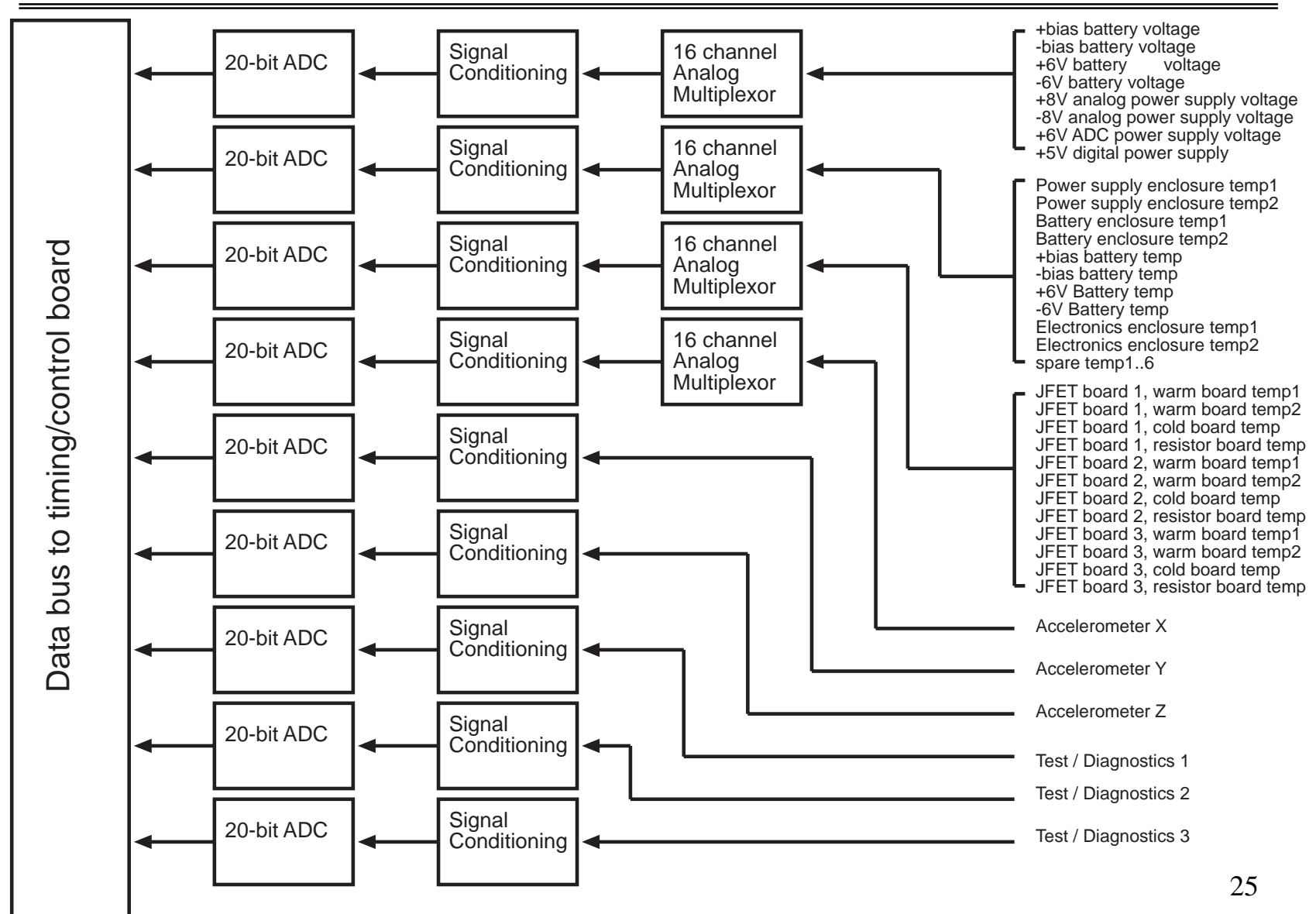
Auxiliary Analog Board



- **Provides signal conditioning and digitization of analog signals**
 - Direct readouts
 - Accelerometers (X, Y, Z)
 - Test and diagnostics channels (3)
 - Multiplexed readouts
 - Power supply voltages
 - Detector electronics enclosure temperatures
 - Battery temperatures
 - JFET warm board temperatures
- **Data conversion**
 - Data sampled synchronously with bolometer data
 - Uses Burr-Brown 20-bit ADCs
- **Physical layout is similar to Preamp/ADC board**
 - Analog portions of board shielded from digital section



Aux. Analog Board





JFET Boards



-
- **JFET temperature control board**
 - Provides control of JFET warm board heaters
 - Analog closed loop control
 - Set point controlled by 16-bit DAC
 - Direct output mode for software control loop
 - Buffers temperature signals for readout by auxiliary analog board
 - **JFET power and detector bias board**
 - Provides stable, low noise sources
 - Bias voltage adjustable in software
 - Digital potentiometer provides 256 step voltage divider
 - Upper and lower voltages adjustable with jumpers
 - Provides ability to generate load curves
 - Option on board to hard jumper output voltage
 - Provides fall back if noise problems with

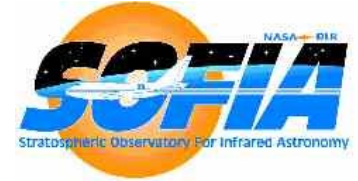


Temperature Control Board





Power Supply & Batteries

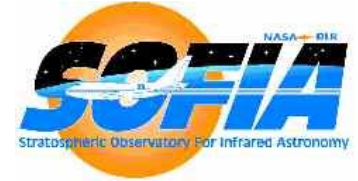


- **Detector electronics power supply box (Cryostat exterior)**
 - AC power
 - Incoming power is fused and filtered
 - Linear power supplies
 - $\pm 8\text{V}$ @ 2.5A (preamps)
 - +6V @ 8A (ADC)
 - +5V @ 3A (digital)

- **Detector electronics battery box (Cryostat exterior)**
 - Components
 - (2) 6V 33Ah sealed lead acid batteries
 - (2) 6V 3Ah sealed lead acid batteries
 - Battery power interruption relay
 - Disconnects batteries when AC power is removed from instrument
 - Runtime estimated at 12-16 hours starting with full charge



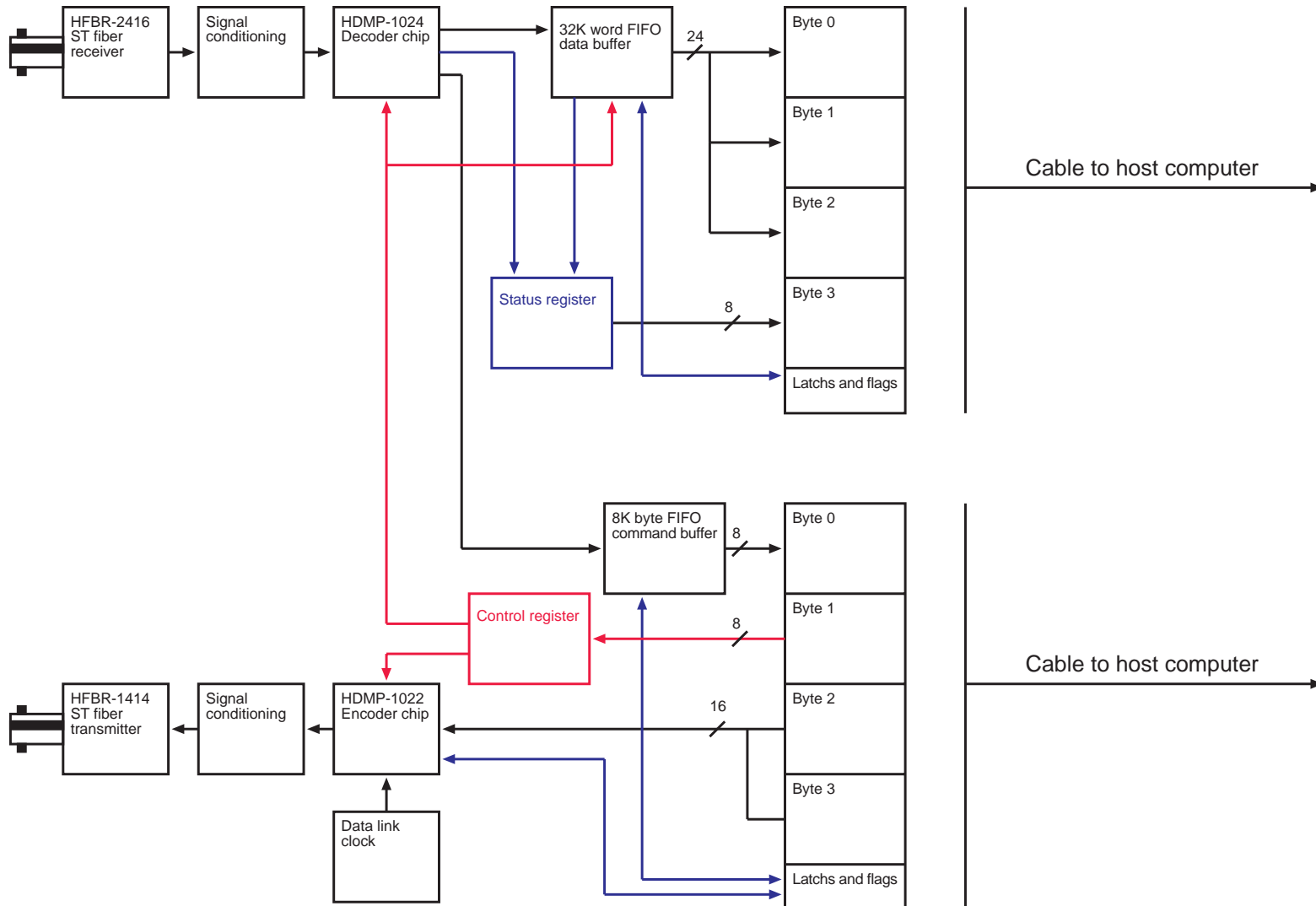
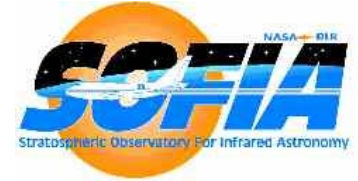
Host Computer Interface



- **Fiber interface**
 - Located in PI rack next to host computer
 - Modified version of fiber board on camera
 - Uses same fiber components
 - Adds 32K word FIFO buffers for incoming data stream
 - Interfaces to host computer through National Instruments DIO-32HS cards
 - One card handles incoming data stream
 - Other card handles commands to electronics
- **Host computer**
 - Baseline design uses Macintosh
 - Requires (2) PCI slots for NI cards
 - Interface to SOFIA LAN through ethernet
 - Can support disk space for raw data storage

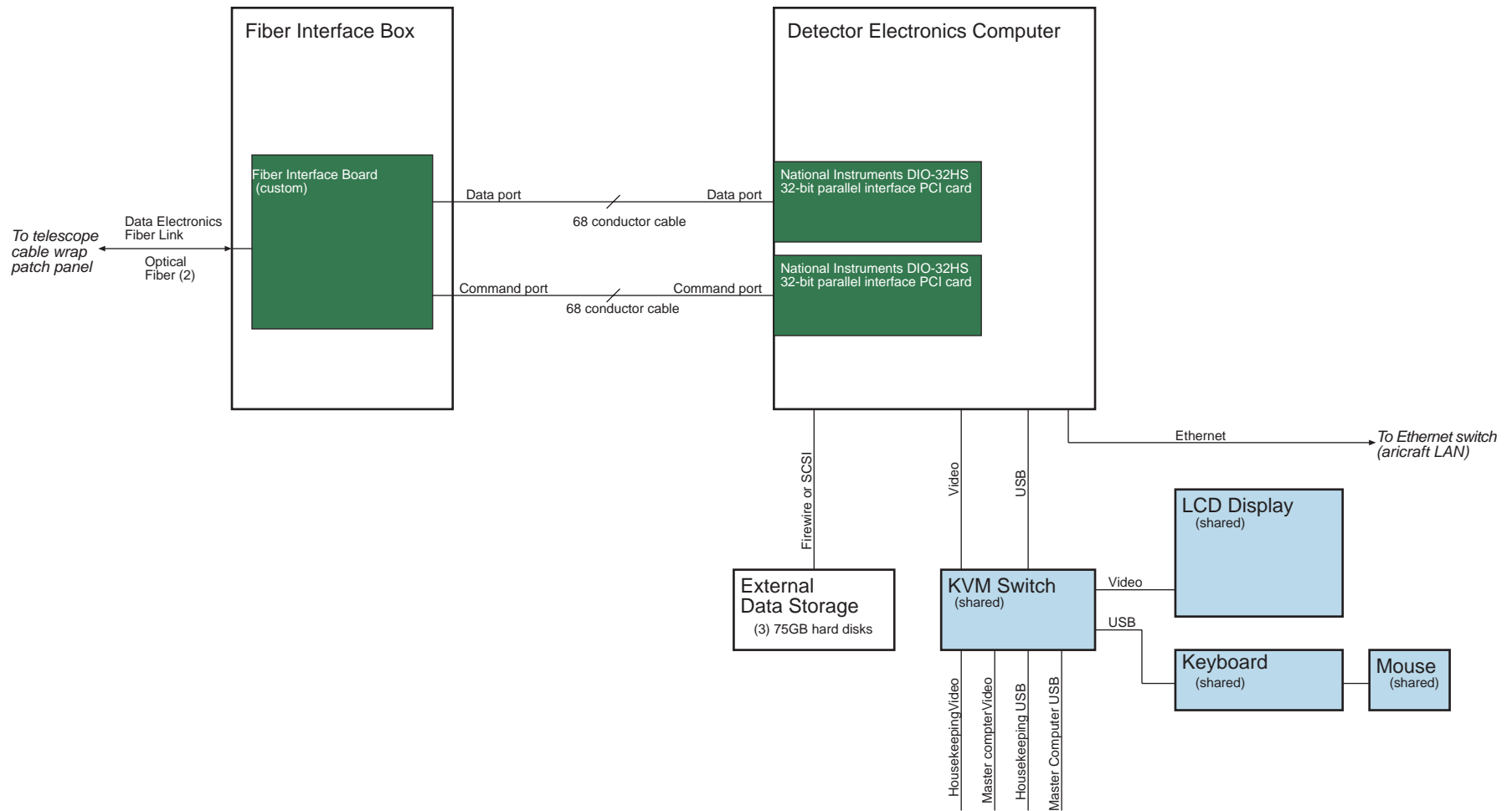


Computer Fiber Interface





Host Computer





Software



-
- **Provides interface between hardware and IRC software**
 - Controls hardware initialization and configuration
 - Adds time stamp to incoming data
 - Buffers data
 - Logs raw data
 - Separates science data and diagnostic data
 - **Data rates**
 - 1.7MBytes/sec raw data at 1KHz sample rate
 - 3.4MBytes/sec raw data at 2KHz sample rate
 - 6.8MBytes/sec raw data at 4KHz sample rate



Software Data Flow

